A 1.25GHz 113fJ 4-bit Absolute-Value Detector for use in Neural Spike Sorting

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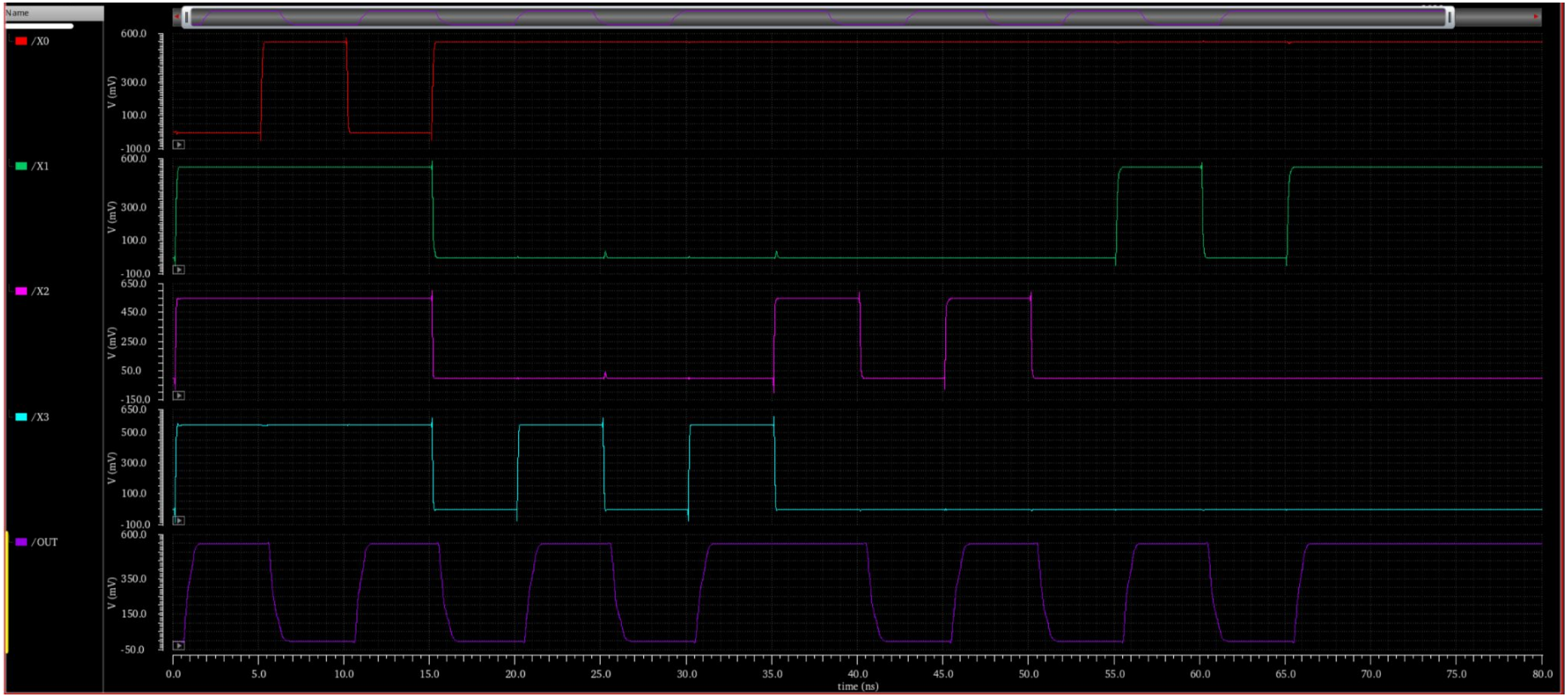
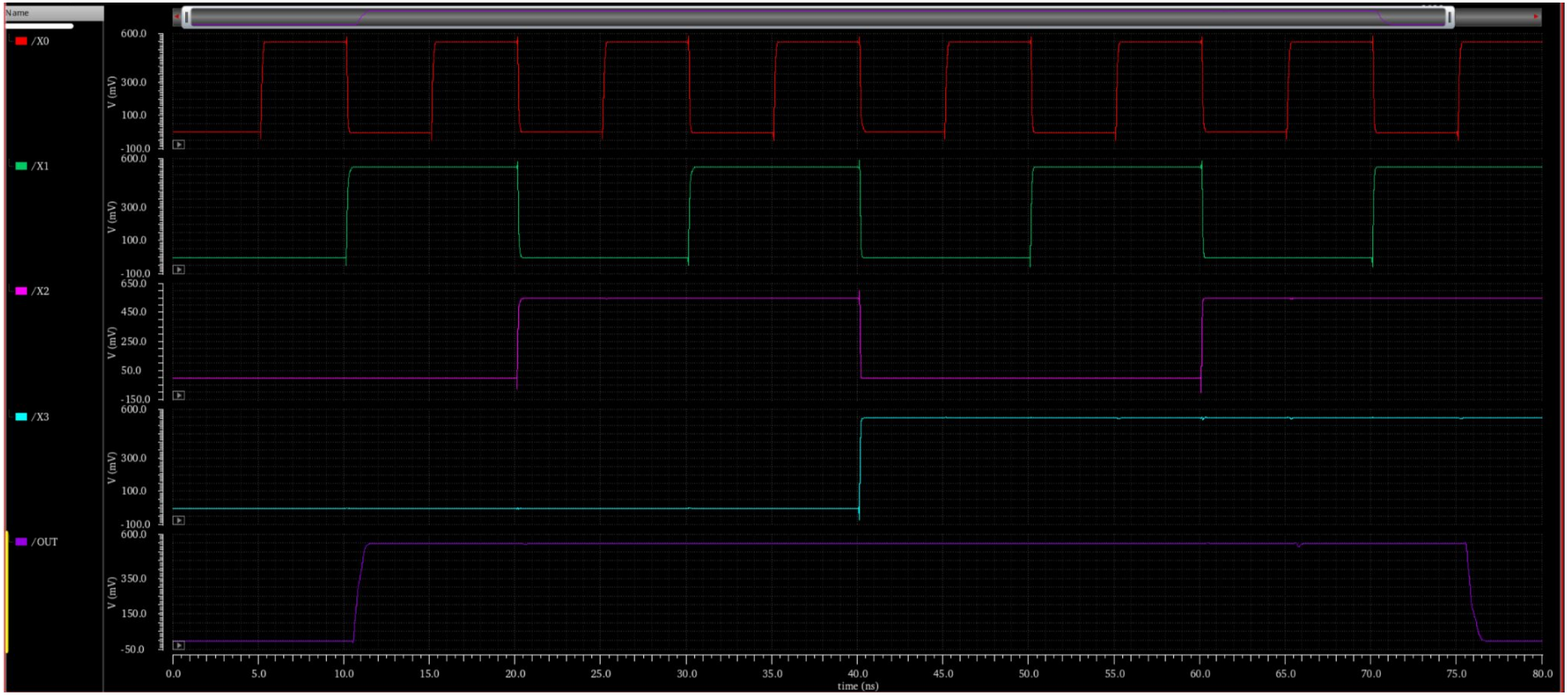
Correctness

Given Testbench (Limited Test Cases):

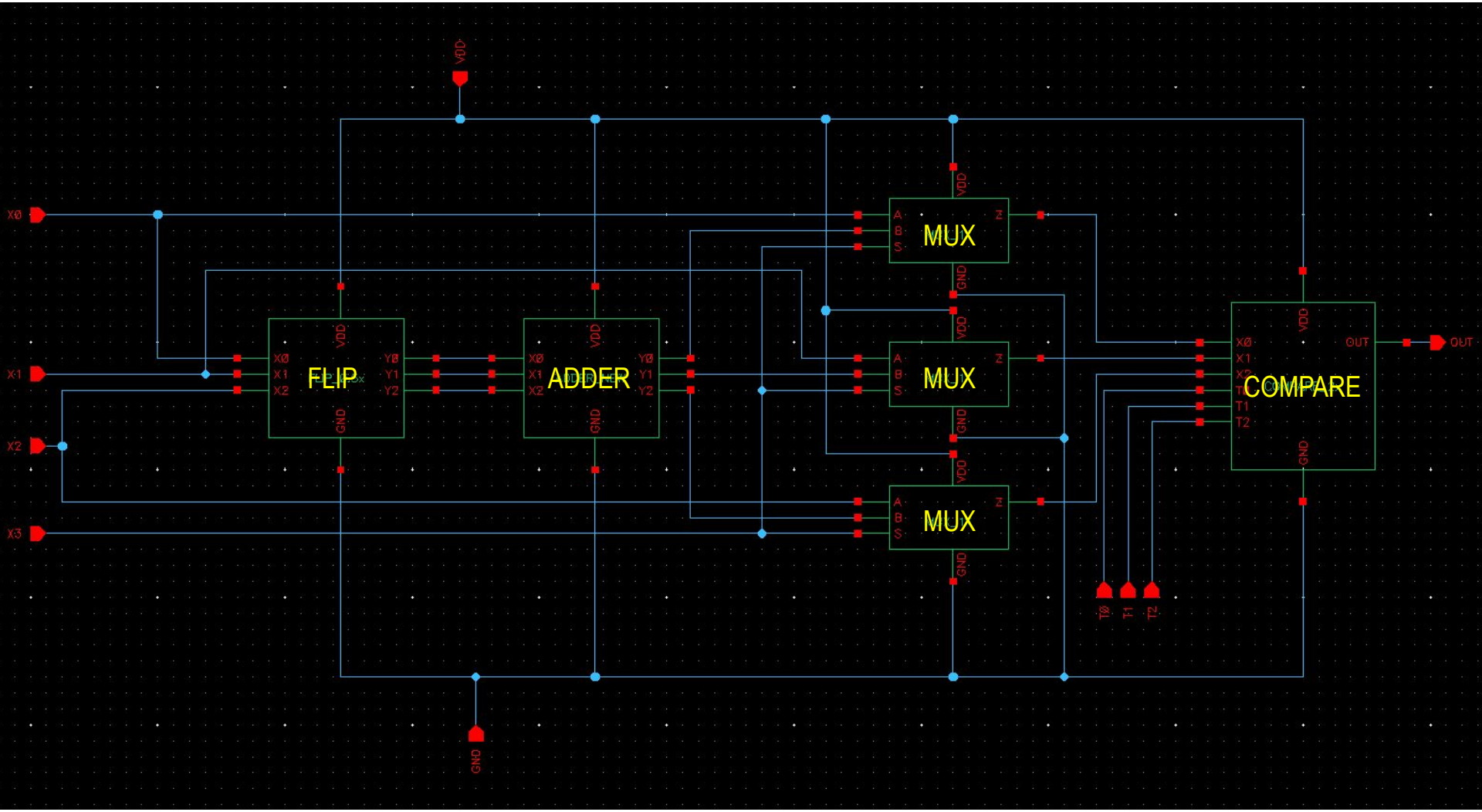


Correctness

Custom Testbench (All Test Cases, Only T=1 Cases Shown):



Old Design Topology



Old Design Results

Performance:

E_0 *(no* V_{DD} *or sizing) = 3638.43fJ*

D_{min} *(no* V_{DD} *or sizing) = 406.451 ps*

E_1 *(*V_{DD} *and sizing) =* ***147.509 fJ***

V_{DD} *=* ***0.5815 V***

ΔE*(Sizing) = 1099.19 fJ - 3638.43 fJ =* ***-2,539.24 fJ***

ΔD*(Sizing) = 309.332 ps - 406.451 ps =* ***-97.119 ps***

$\Delta E(V_{DD})$ *= 470.453 fJ - 3638.43 fJ =* ***-3,167.977 fJ***

$\Delta D(V_{DD})$ *= 725.212 ps - 406.451 ps =* ***+318.761 ps***

Old Design Issues

1. ***Be careful with PTL***

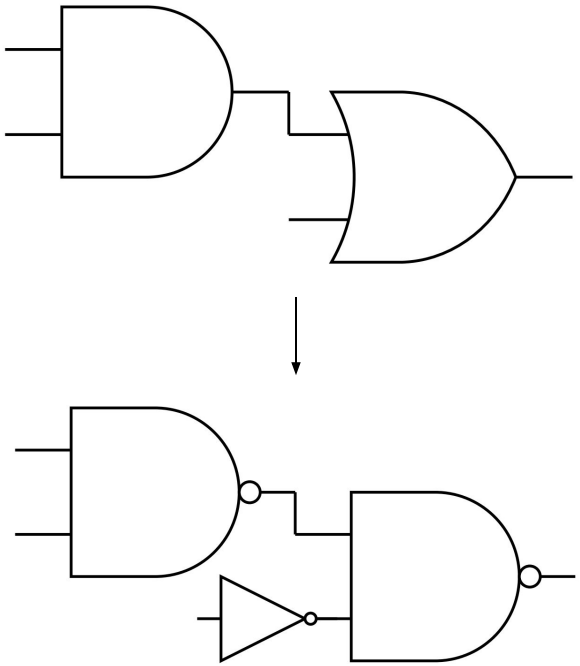
- *PTL AND used in adder*
- *Output not full swing*
- *Correctness affected*
- *Swtich to CMOS instead (utilized in new design)*

2. ***The default Virtuoso library gates are not sized to match unit inverter by default***

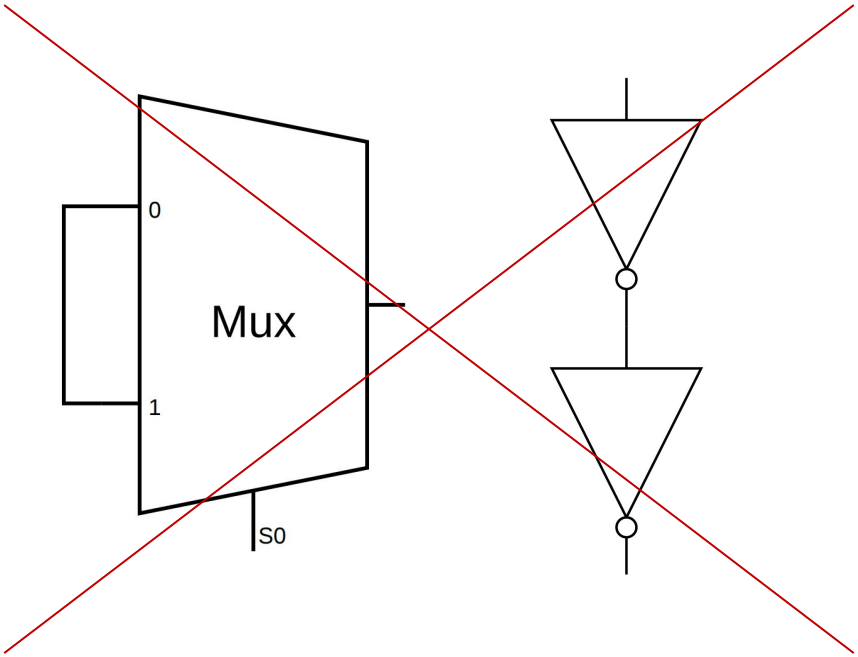
Fortunately, we later find out it is not useful anyway…

Circuit Topology Optimization

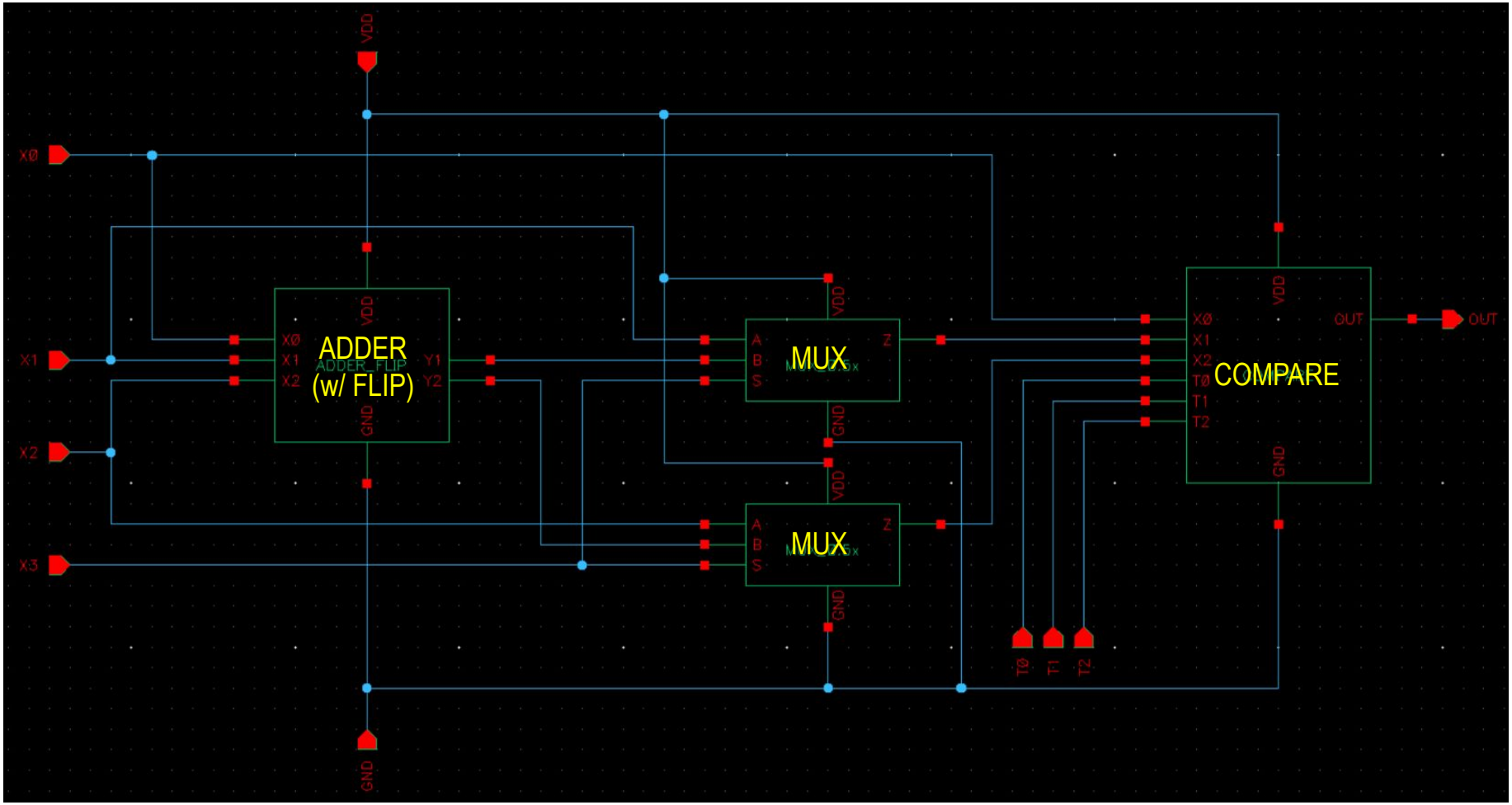
- **NAND/NOR minimization for boolean logic**
  - Minimize number of gates



- **Removal of redundant logic and gates**
  - double inverter
  - meaningless multiplexer

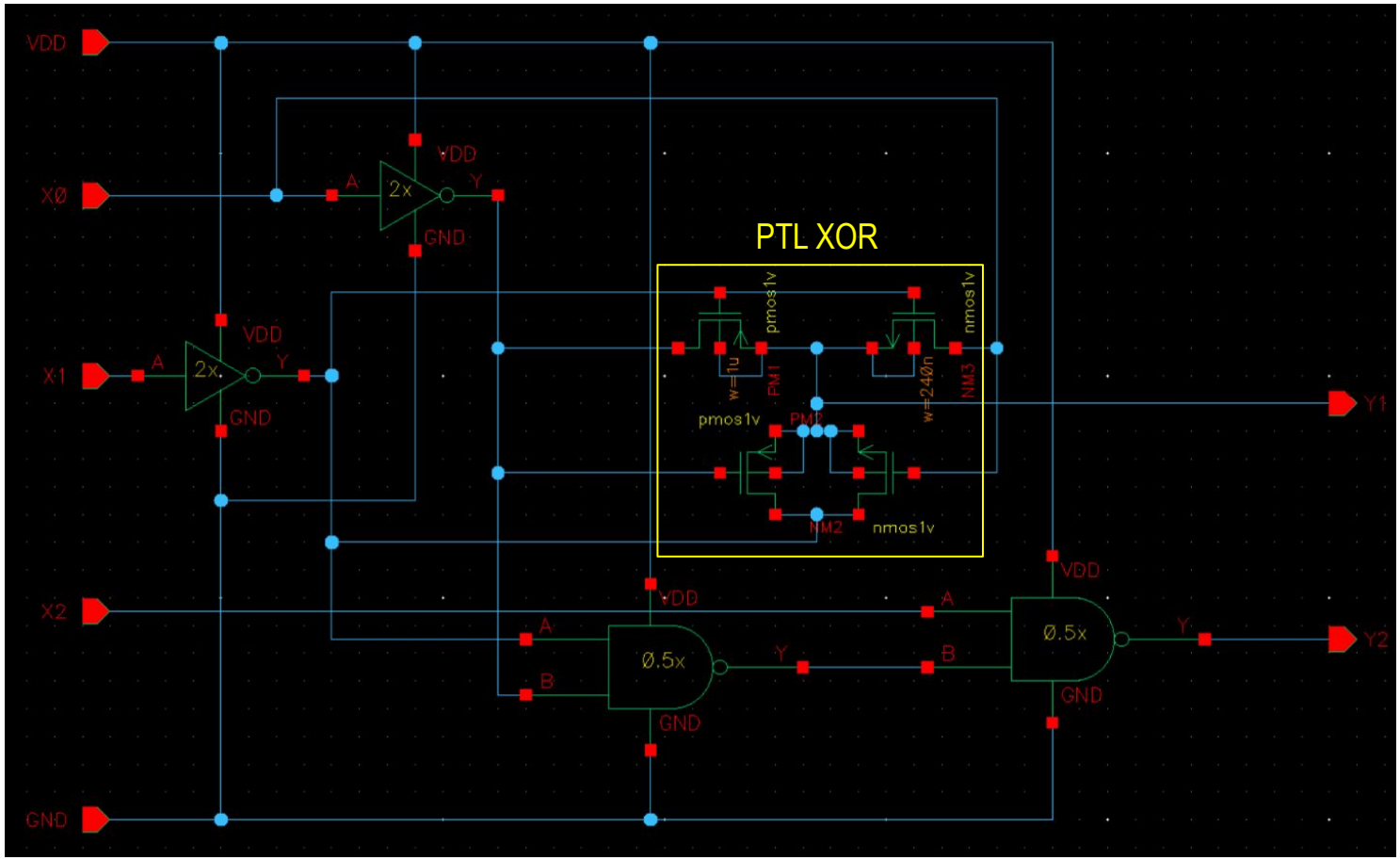


New Design Topology



New Design Topology

- Combining FLIP and ADDER (with optimization)



New Design Results

Performance:

E_0 (no V_{DD}) = 1586.55 fJ

D_{min} (no V_{DD}) = 225.173 ps

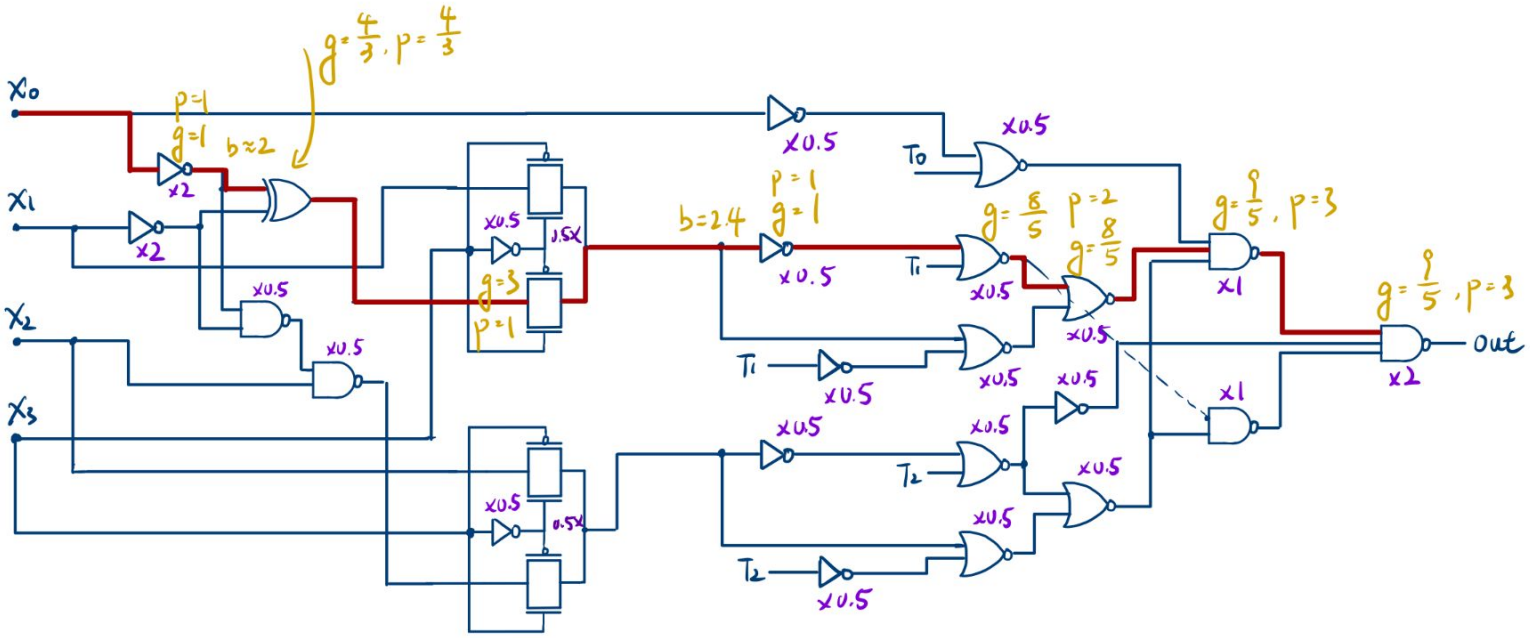
E_1 (V_{DD}) = 113.807 fJ ~34 fJ reduction from old design

V_{DD} = 0.551 V

$\Delta E(V_{DD})$ = 113.807 fJ - 1586.55 fJ = -1472.743 fJ

$\Delta D(V_{DD})$ = 671.151 ps - 225.173 ps = +445.978 ps

Critical Path Analysis



$$\text{Delay} = \frac{X_1}{5} + 1 + \frac{X_2}{X_1}\cdot 2 + 1 + \frac{X_3}{X_2}\cdot\frac{4}{3} + \frac{4}{3} + \frac{X_4}{X_3}\cdot 3\cdot 2.4 + 1 + \frac{X_5}{X_4} + 1 + \frac{X_6}{X_5}\cdot\frac{8}{5} + 2$$
$$+ \frac{X_8}{X_7}\cdot\frac{8}{5} + 2 + \frac{X_9}{X_8}\cdot\frac{9}{5} + 3 + \frac{32\times 5}{X_9}\cdot\frac{9}{5} + 3$$

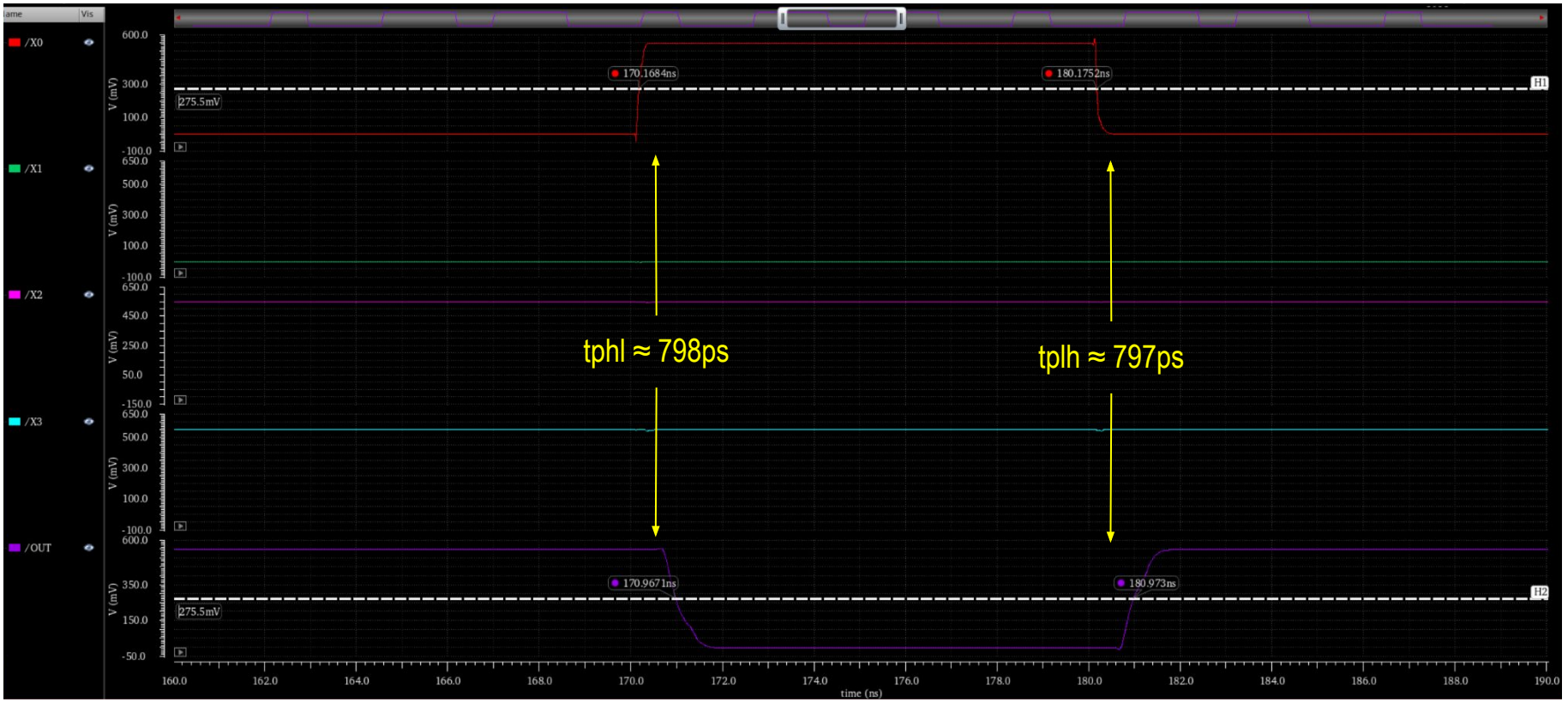
Matlab results

1	12.9088
2	16.6637
3	32.2663
4	11.5700
5	29.8709
6	48.1995
7	77.7743
8	111.5530

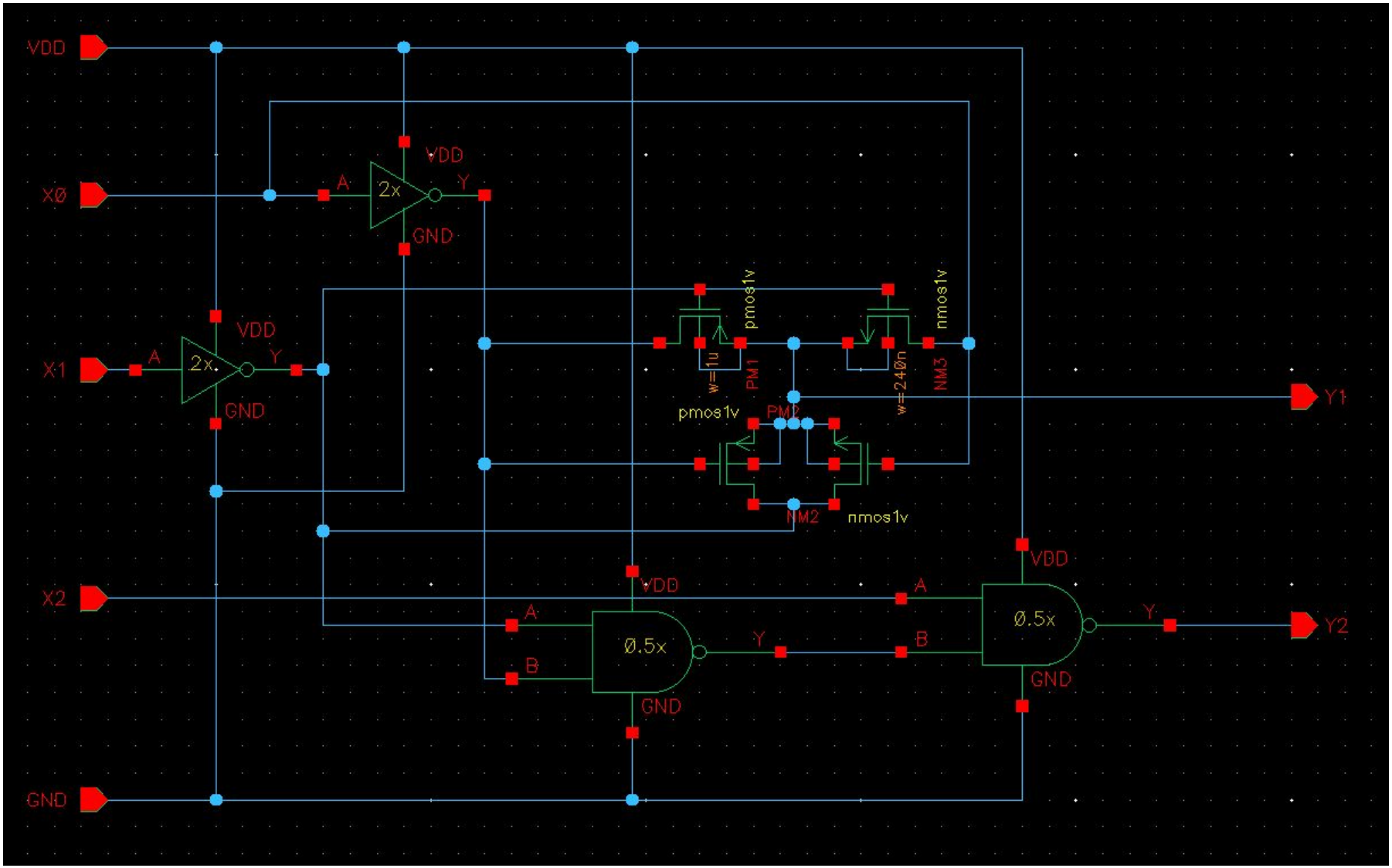
Critical Path Analysis

Worst two cases:

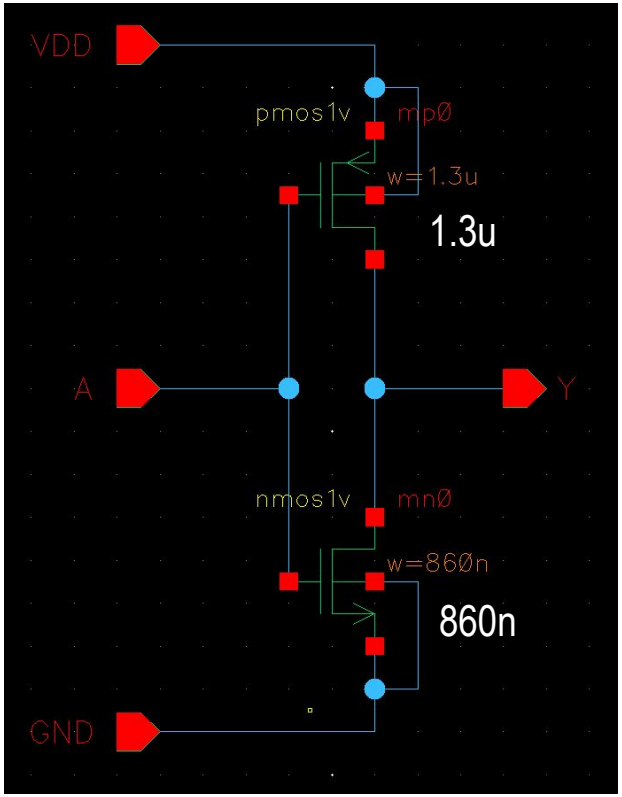
1. **x0 triggered tphl: 1101 -> 1100 ~798ps @0.551V**
2. **x0 triggered tplh: 1100 -> 1101 ~797ps @0.551V**

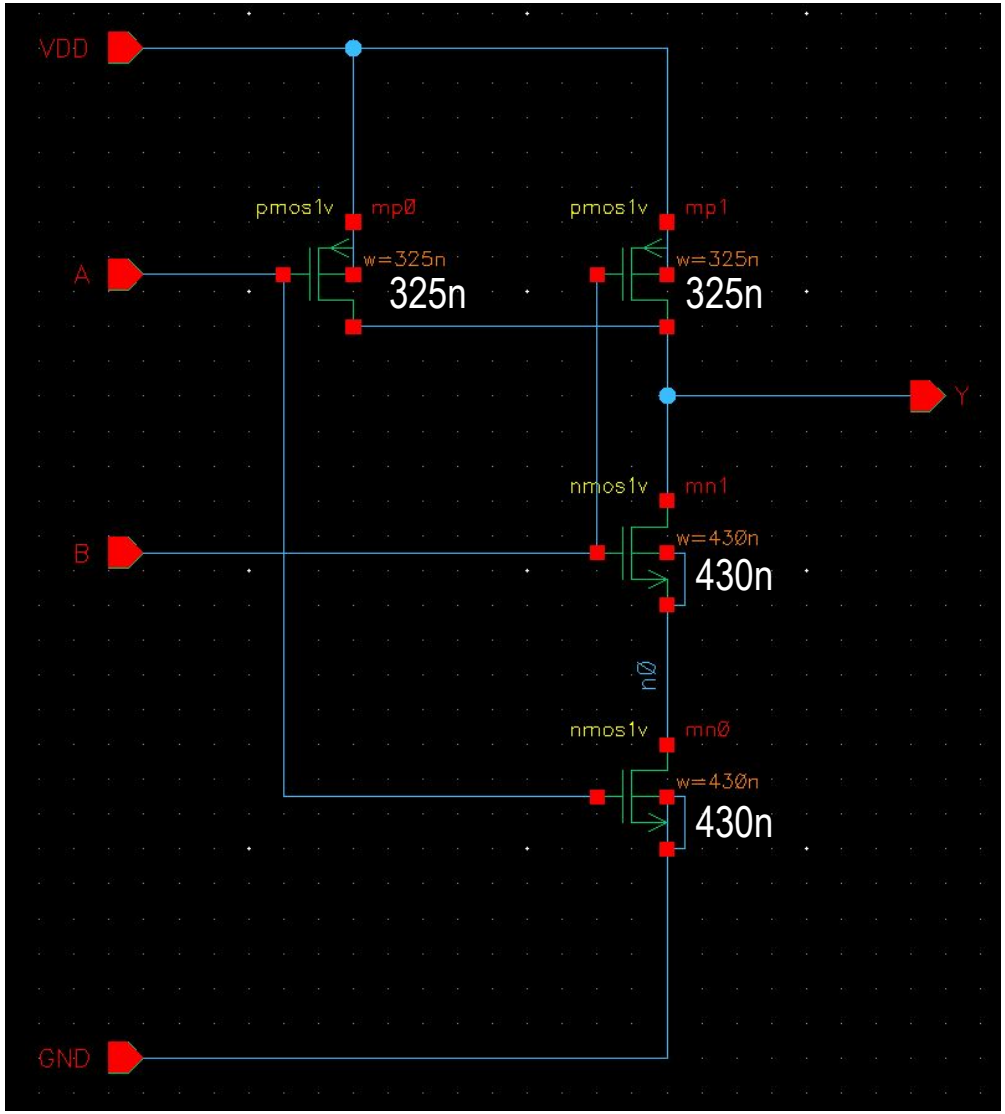


Gate Sizing (Adder)

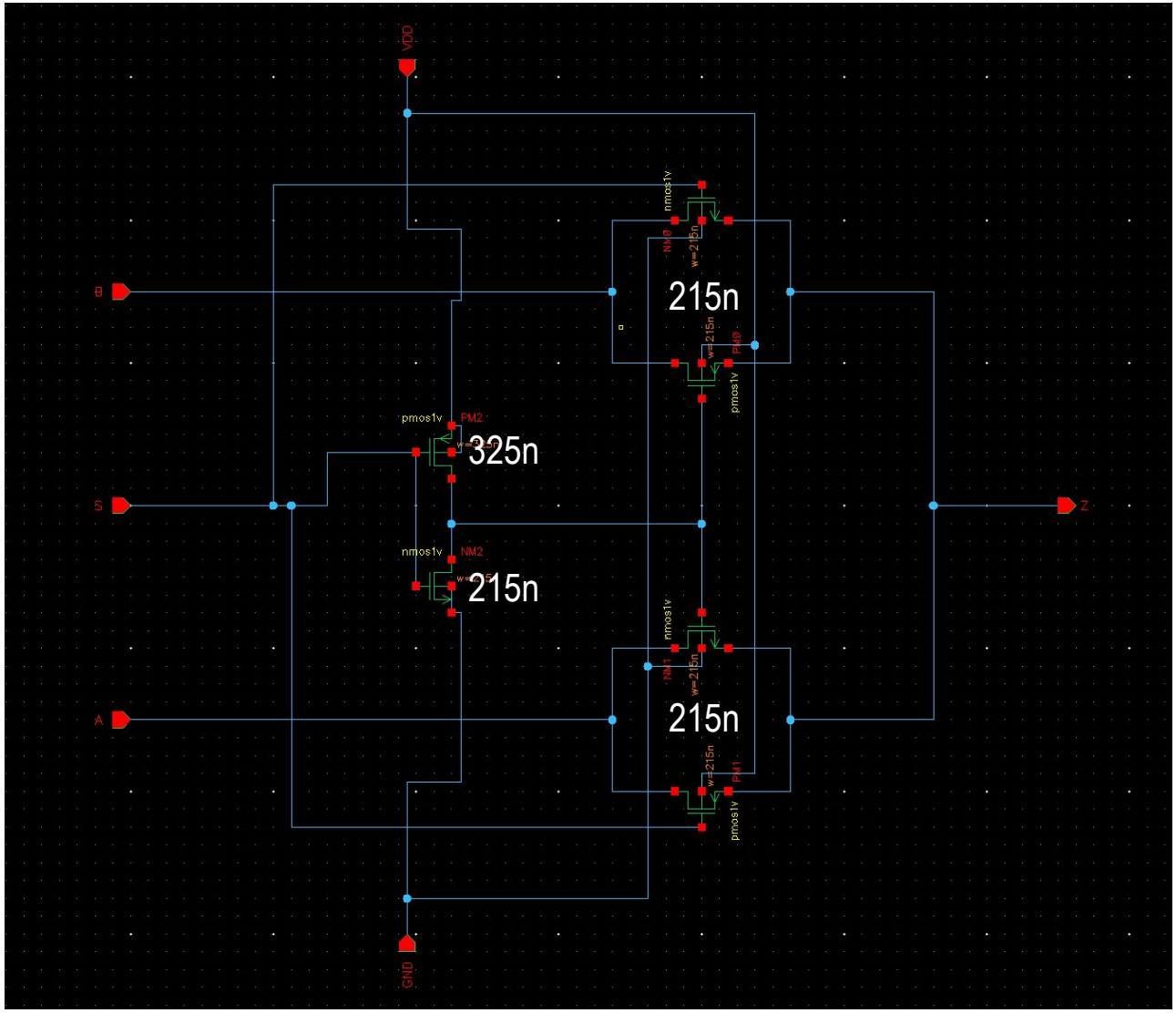


Gate Sizing (Adder)

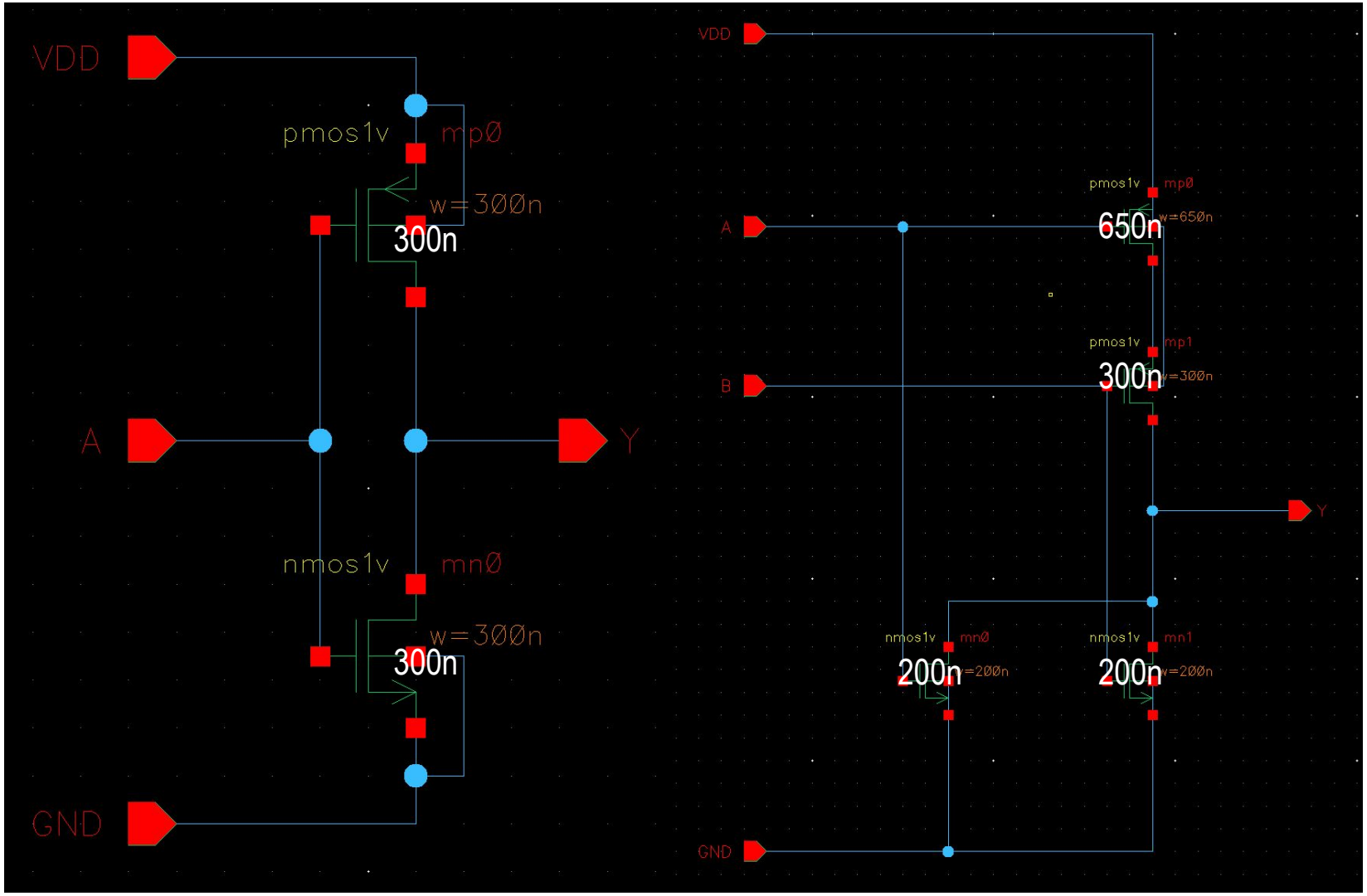




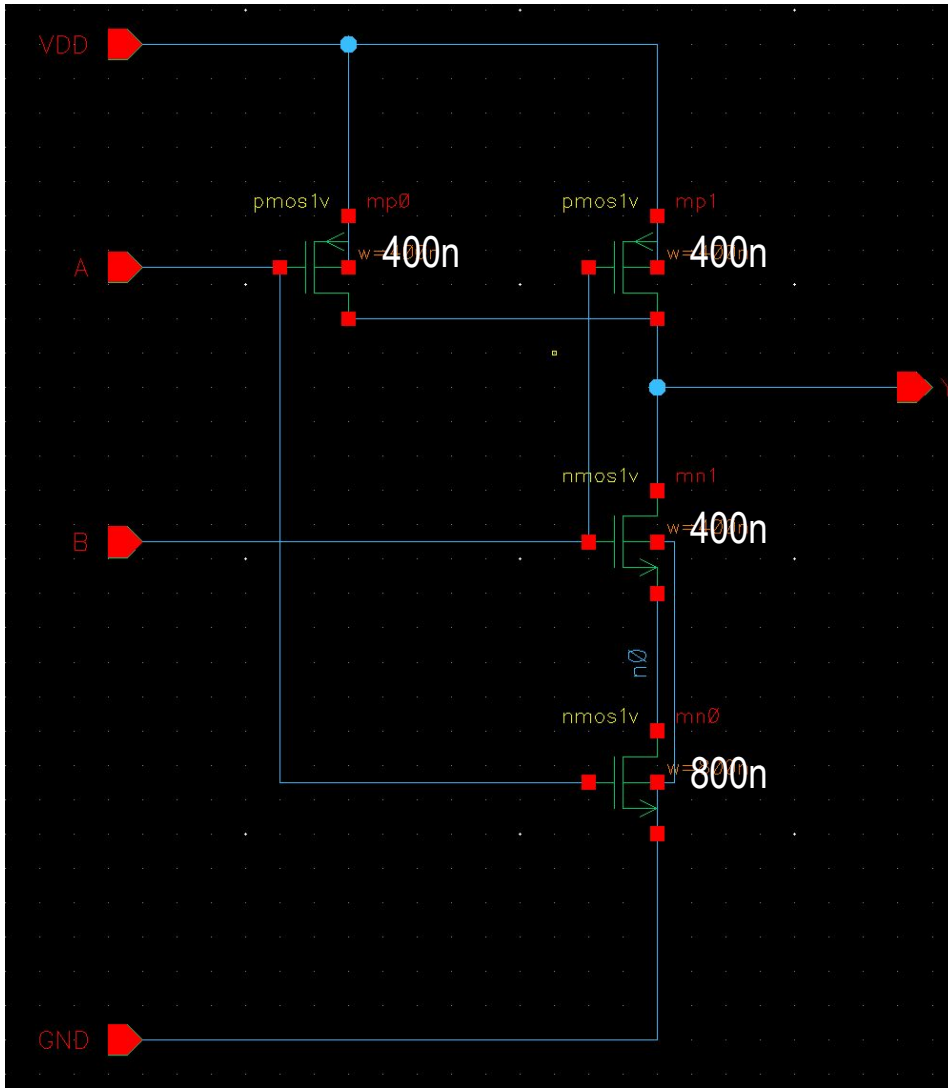
Gate Sizing (MUX)



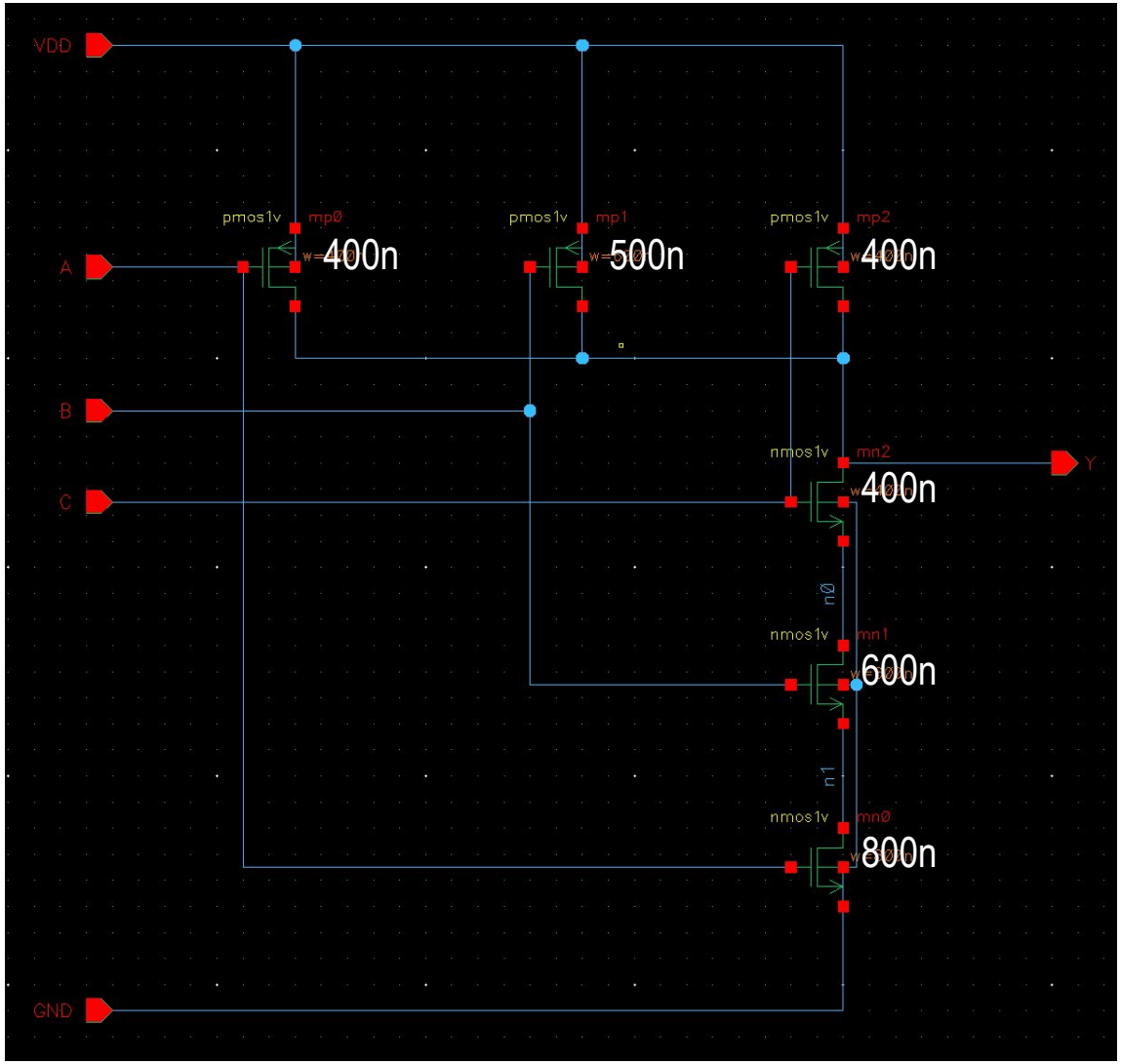
Gate Sizing (Comparator)



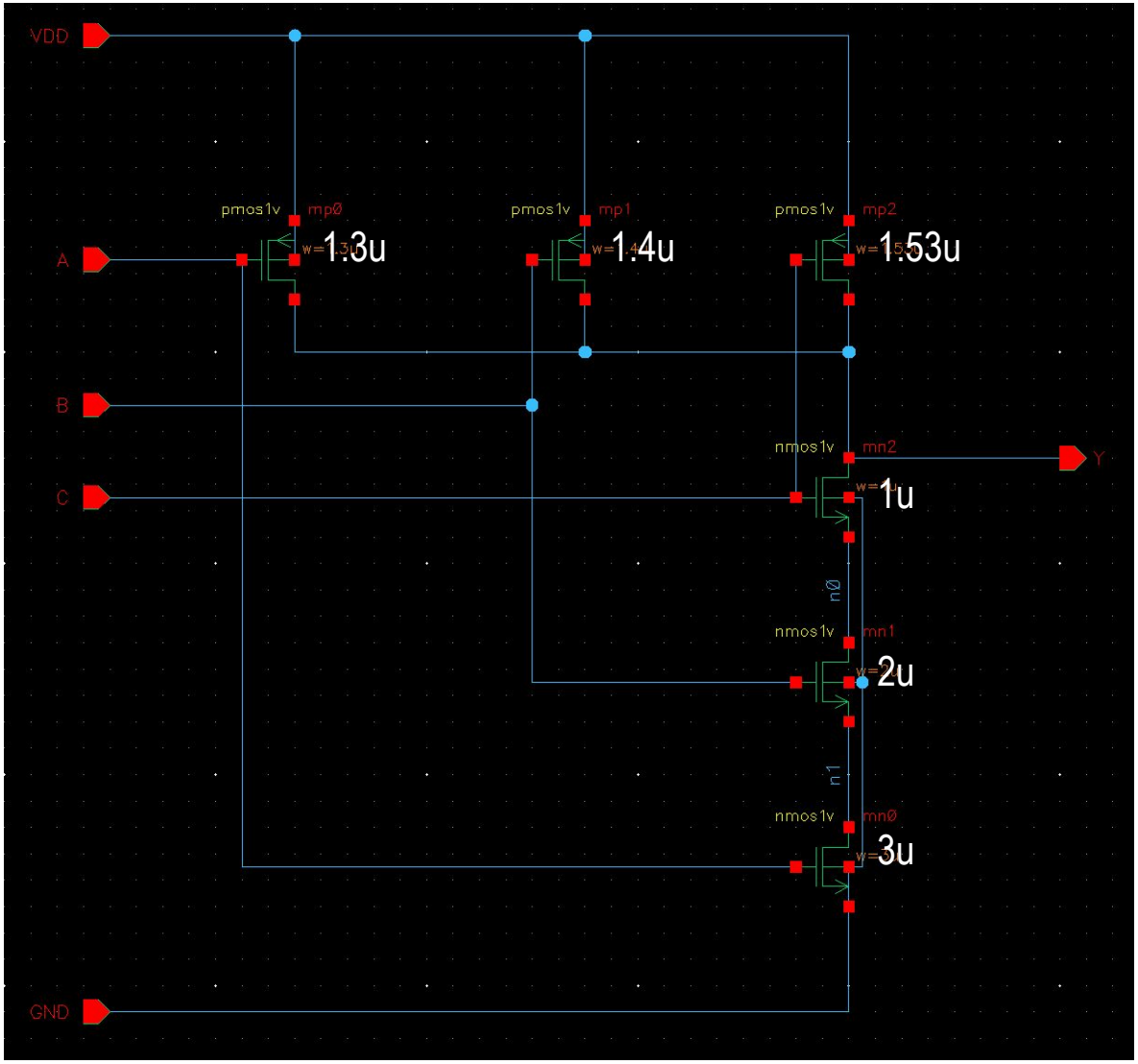
Gate Sizing (Comparator 2-input Nand 1x)



Gate Sizing (Comparator 3-input Nand 1x)

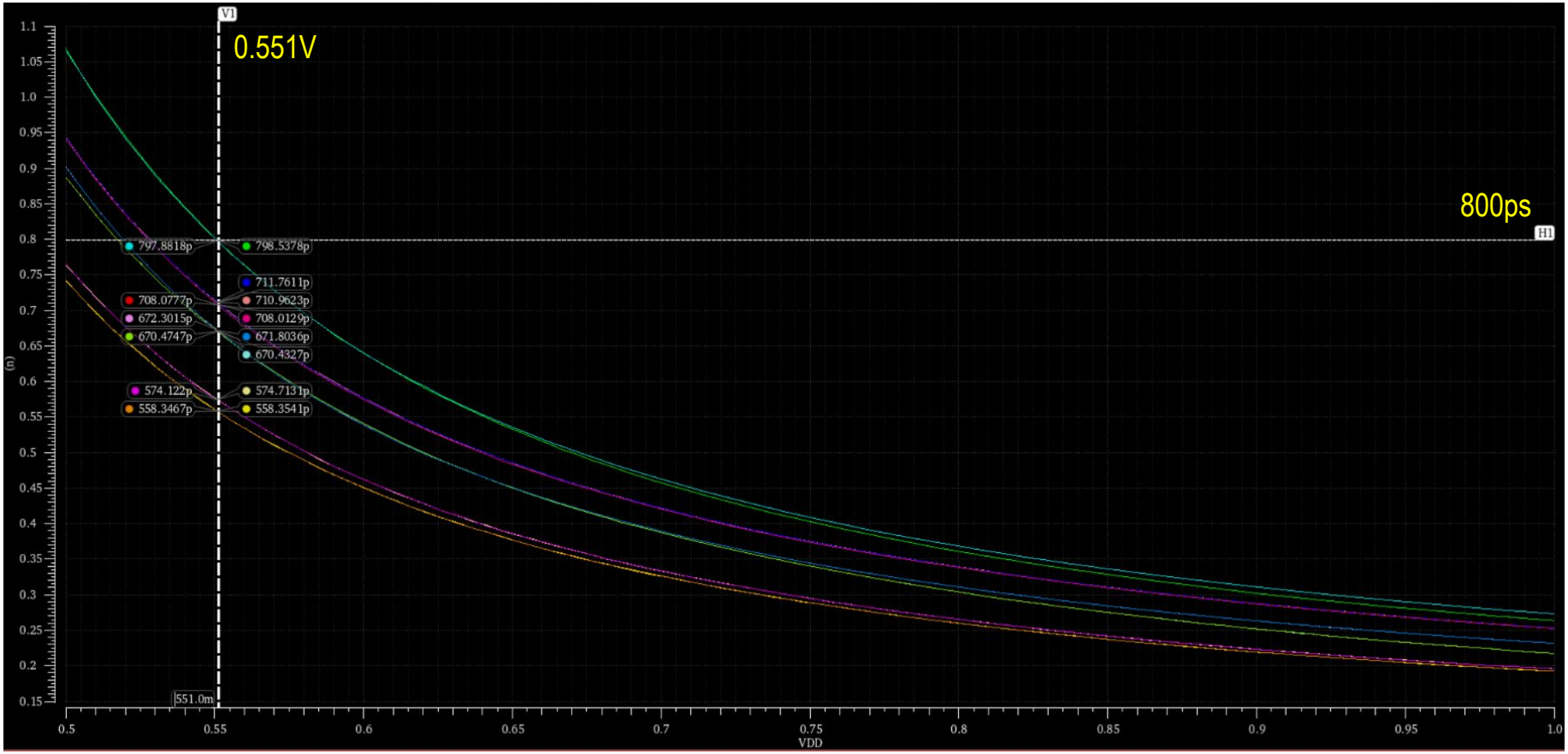


Gate Sizing (Comparator 3-input Nand 2x)



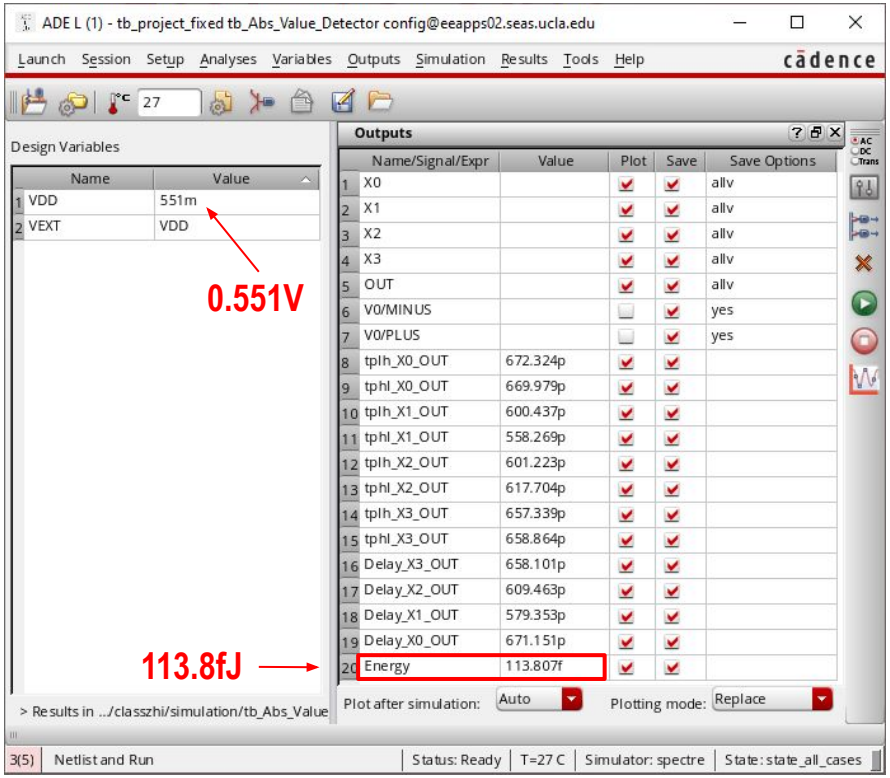
Design Optimization (V_{DD})

- Best V_{DD} determined according to worst case t_p of critical path

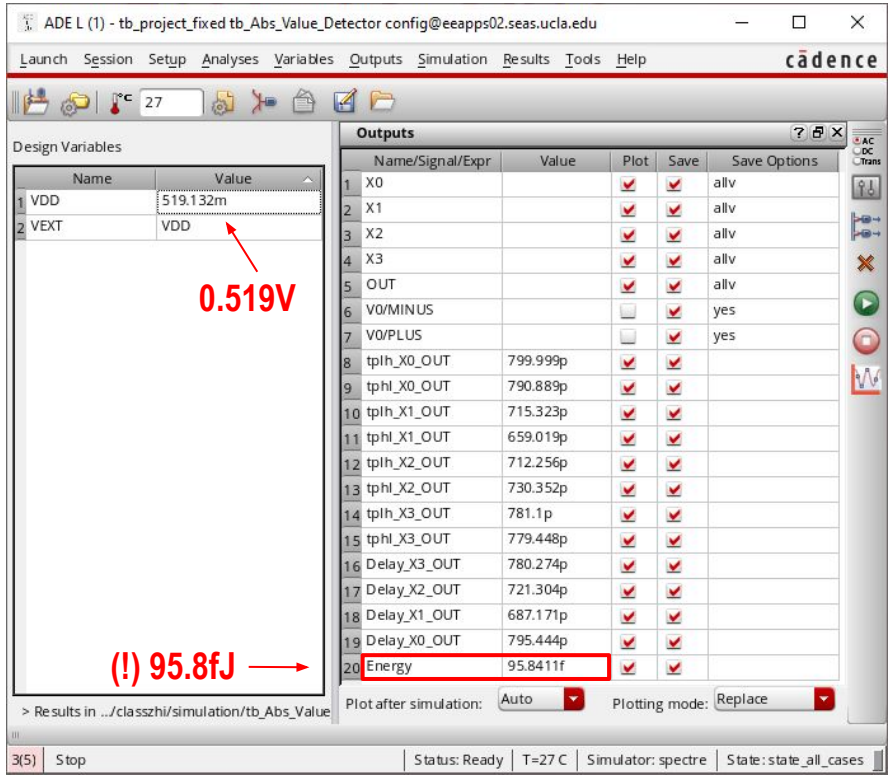


Design Optimization (V_{DD})

- **Simulation results (delay and energy)**



VDD scaled according to actual worst case



VDD scaled according to given testbench

ECE115C Final Project

Thanks for listening! ヾ(•ω•*)