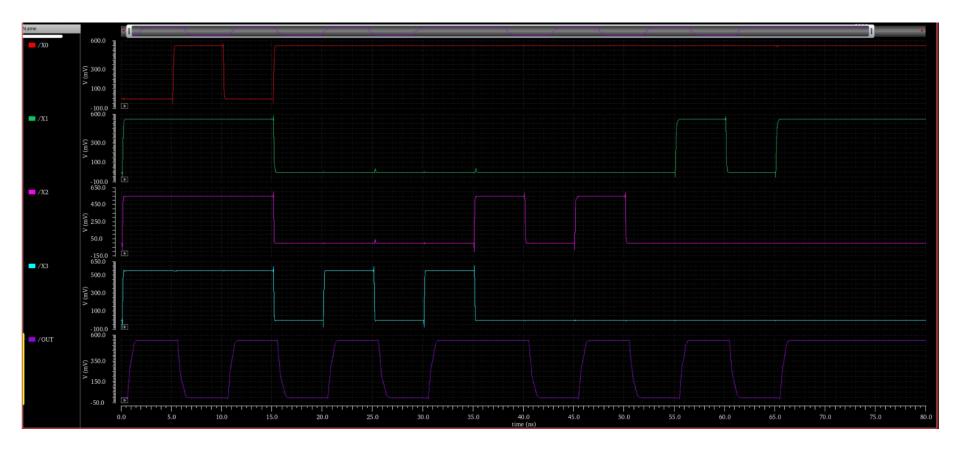
A 1.25GHz 113fJ 4-bit Absolute-Value Detector for use in Neural Spike Sorting

Jack Zhi 605167402 Siwei Yuan 005321623 Young He 205417200



Correctness

Given Testbench (Limited Test Cases):

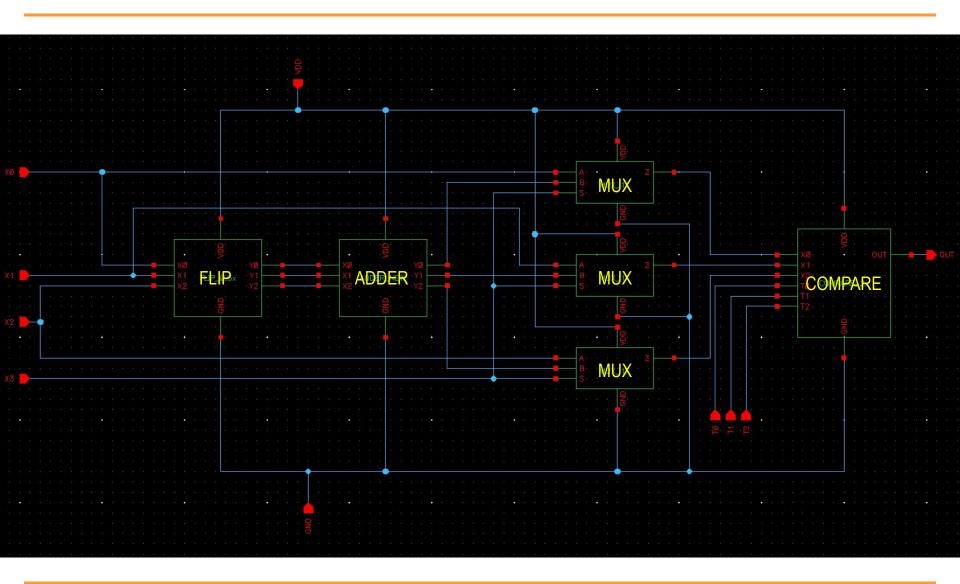


Correctness

Custom Testbench (All Test Cases, Only T=1 Cases Shown):



Old Design Topology



UCLA

Performance:

$$\begin{split} &E_0 \ (no \ V_{DD} \ or \ sizing) = 3638.43 fJ \\ &D_{min} \ (no \ V_{DD} \ or \ sizing) = 406.451 \ ps \\ &E_1 \ (V_{DD} \ and \ sizing) = 147.509 \ fJ \\ &V_{DD} = \underline{0.5815 \ V} \\ &\Delta E(Sizing) = 1099.19 \ fJ - 3638.43 \ fJ = -2,539.24 \ fJ \\ &\Delta D(Sizing) = 309.332 \ ps - 406.451 \ ps = -97.119 \ ps \\ &\Delta E(V_{DD}) = 470.453 \ fJ - 3638.43 \ fJ = -3,167.977 \ fJ \\ &\Delta D(V_{DD}) = 725.212 \ ps - 406.451 \ ps = +318.761 \ ps \end{split}$$

Old Design Issues

1. Be careful with PTL

- PTLAND used in adder
- Output not full swing
- Correctness affected
- Swtich to CMOS instead (utilized in new design)

2. The default Virtuoso library gates are not sized to match unit inverter by default

Fortunately, we later find out it is not useful anyway...

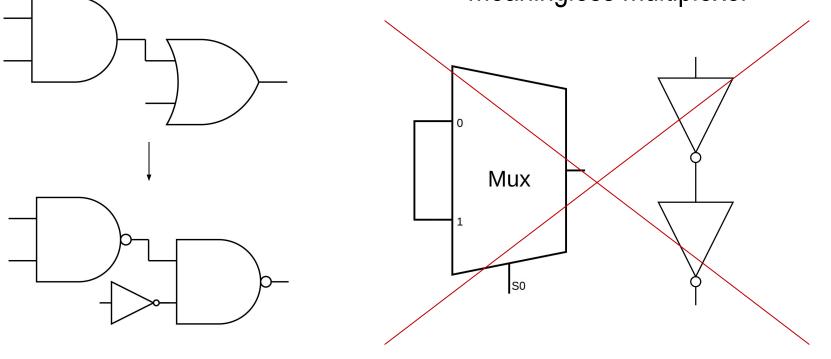
Circuit Topology Optimization

NAND/NOR minimization for boolean logic

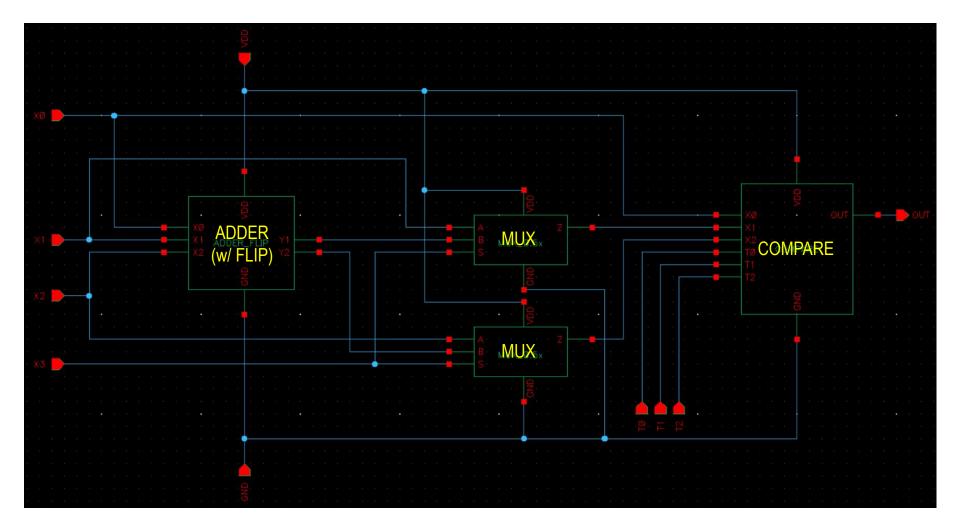
- Minimize number of gates

Removal of redundant logic and gates

- double inverter
- meaningless multiplexer

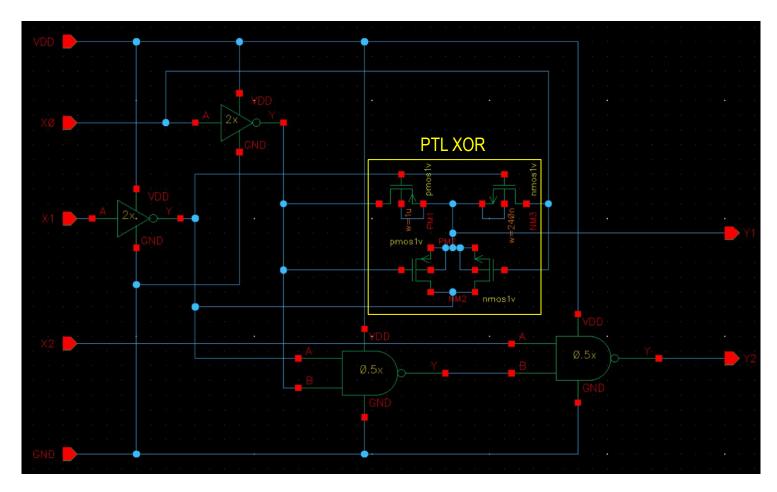


New Design Topology



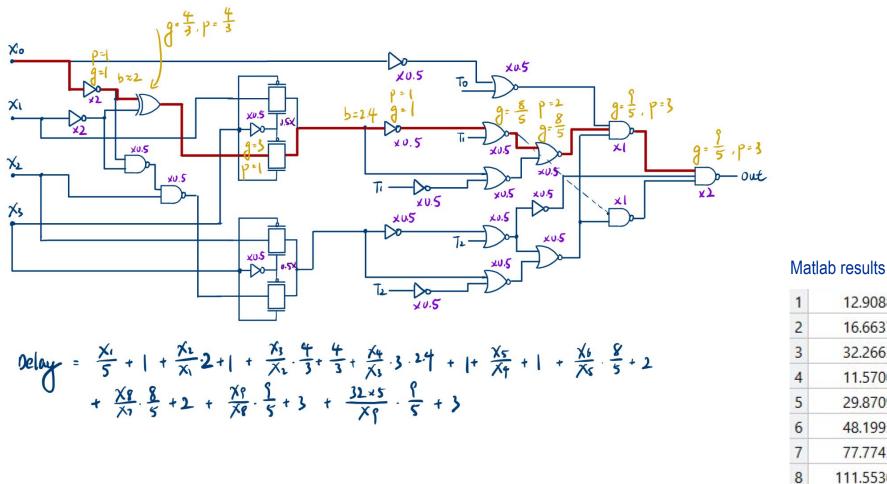
New Design Topology

Combining FLIP and ADDER (with optimization)



$\begin{array}{l} \underline{Performance:} \\ E_{0} \ (no \ V_{DD}) = 1586.55 \ fJ \\ D_{min} \ (no \ V_{DD}) = 225.173 \ ps \\ E_{1} \ (V_{DD}) = \underline{113.807 \ fJ} \quad \sim 34 \ fJ \ reduction \ from \ old \ design \\ V_{DD} = \underline{0.551 \ V} \\ \Delta E(V_{DD}) = 113.807 \ fJ - 1586.55 \ fJ = -1472.743 \ fJ \\ \Delta D(V_{DD}) = 671.151 \ ps - 225.173 \ ps = +445.978 \ ps \end{array}$

Critical Path Analysis



12.9088

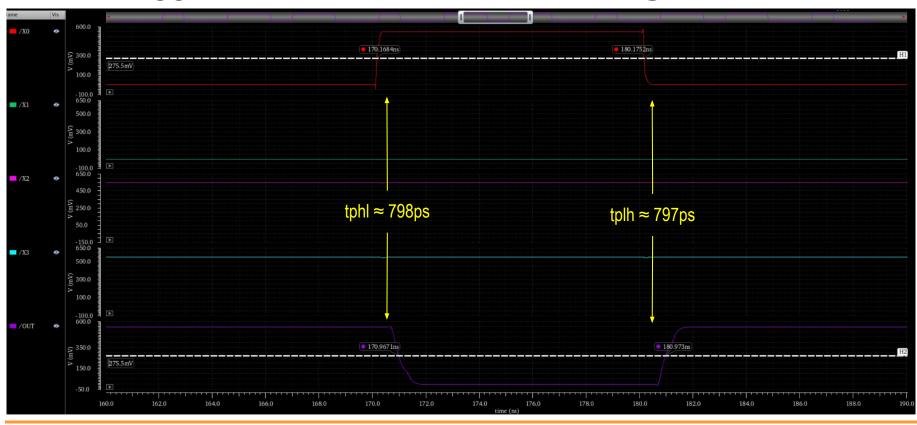
16.6637

32.2663

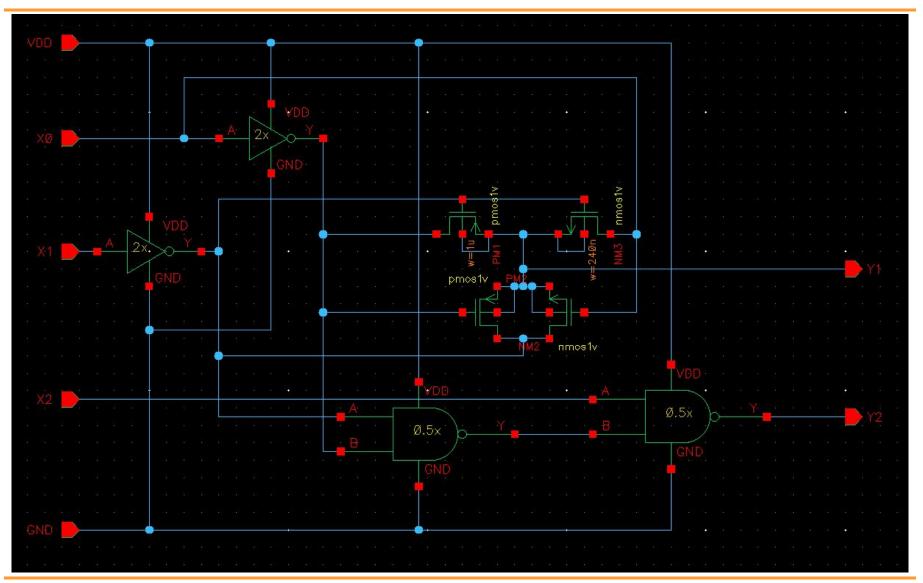
Critical Path Analysis

Worst two cases:

- 1. x0 triggered tphl: 1101 -> 1100 ~798ps @0.551V
- 2. x0 triggered tplh: 1100 -> 1101 ~797ps @0.551V



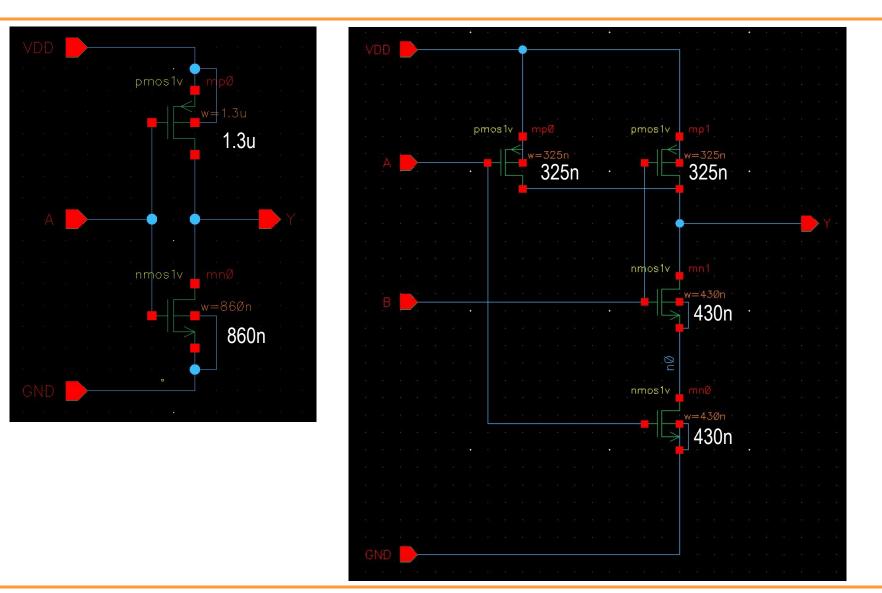
Gate Sizing (Adder)



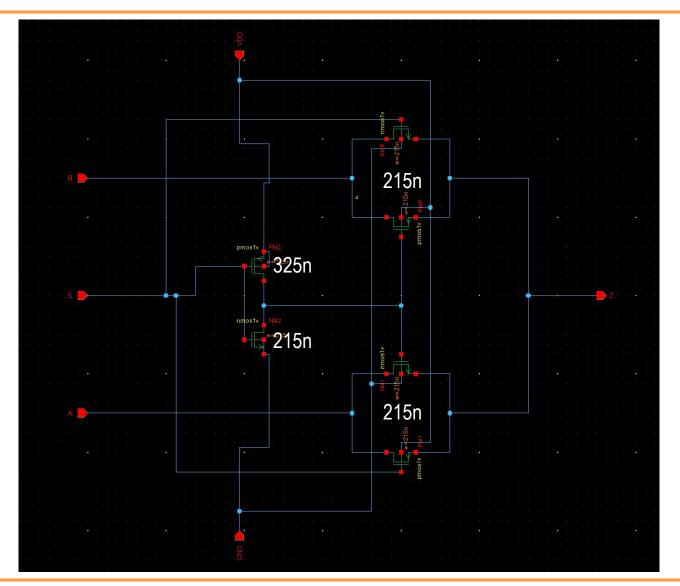
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Gate Sizing (Adder)

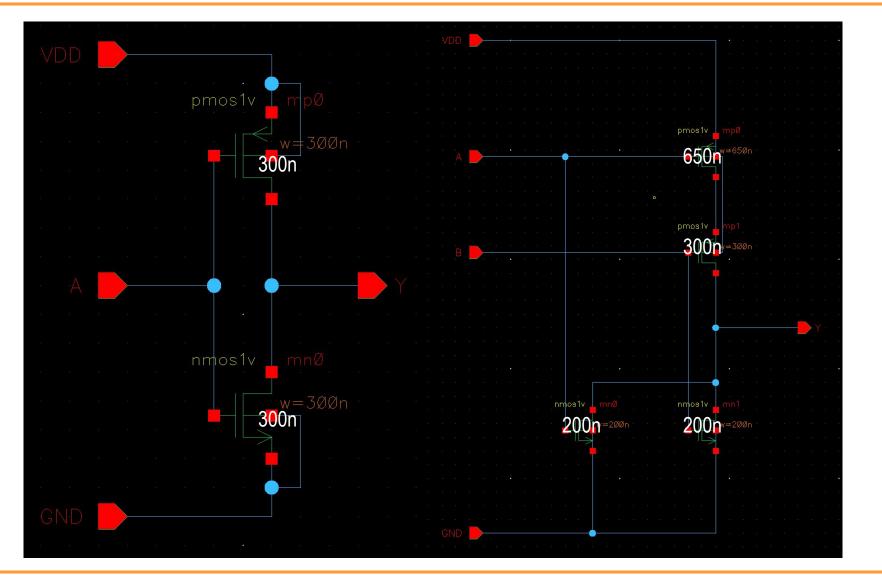


Gate Sizing (MUX)

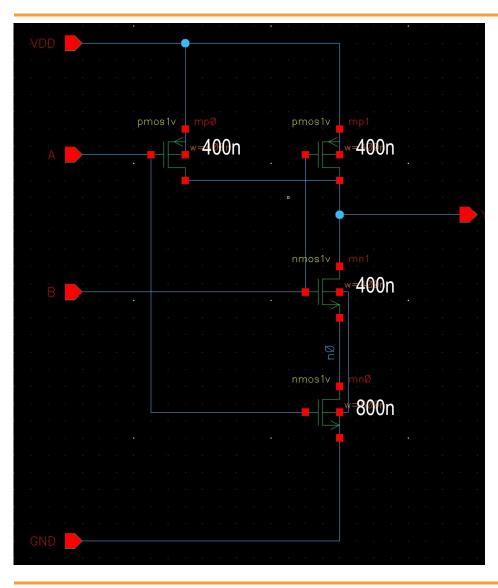


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Gate Sizing (Comparator)

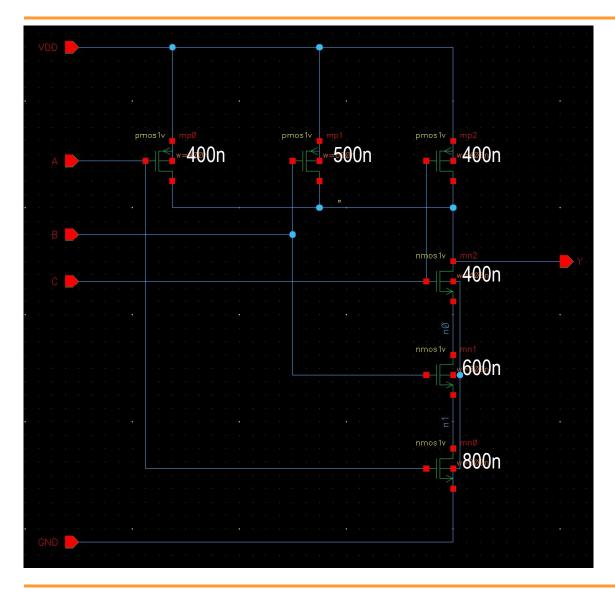


Gate Sizing (Comparator 2-input Nand 1x)



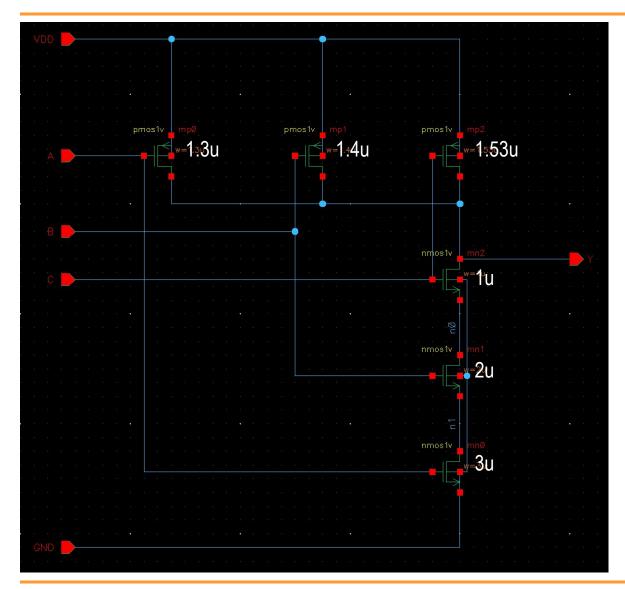


Gate Sizing (Comparator 3-input Nand 1x)



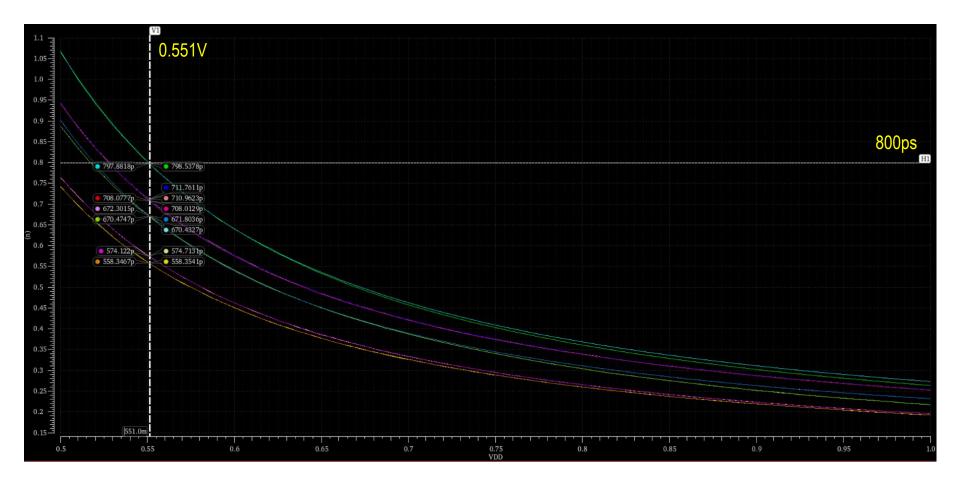
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Gate Sizing (Comparator 3-input Nand 2x)



Design Optimization (V_{DD})

Best V_{DD} determined according to worst case t_p of critical path



Design Optimization (V_{DD})

Simulation results (delay and energy)

| 100 - 1 · | 27 🛛 👌 🎾 🖞 | | | | _ | _ | | |
|------------------|------------|-----|------------------------|----------|---------|----------------------------------|----------------------|-----|
| Design Variables | | | Outputs ? | | | | | |
| Name | Value | T L | Name/Signal/Expr X0 | Value | Plot | Save | Save Options allv | |
| VDD | 551m | | X1 | | | ✓ ✓ | ally | - [|
| VEXT | VDD | 2 | X2 | | ¥ | × | ally | |
| | | 3 | X3 | | × | × | ally | - 2 |
| | | 5 | OUT | | | - | ally | _ |
| 0.551V | | 5 | V0/MINUS | | | × | yes | - (|
| | | 7 | V0/PLUS | | | | yes | - / |
| | | 8 | tplh X0 OUT | 672.324p | | | | - (|
| | | 9 | | 669.979p | | | | |
| | | 1 | 0 tplh_X1_OUT | 600.437p | ¥ | | 0 | |
| | | 1 | 1 tphl_X1_OUT | 558.269p | | | | - |
| | | 1 | 2 tplh_X2_OUT | 601.223p | | | 6 | |
| | | 1 | 3 tphl_X2_OUT | 617.704p | | | | - |
| | | 1 | 4 tplh_X3_OUT | 657.339p | | | | |
| | | 1 | 5 tphl_X3_OUT | 658.864p | | ¥ | | |
| | | 1 | 6 Delay_X3_OUT | 658.101p | | | 5 | |
| | | 1 | 7 Delay_X2_OUT | 609.463p | | ¥ | | |
| | | 1 | 8 Delay_X1_OUT | 579.353p | | | | |
| | 113.8fJ — | 1 | 9 Delay_X0_OUT | 671.151p | | ¥ | | |
| | | | c Energy | 113.807f | × | | | |

VDD scaled according to actual worst case

| 💾 🧬 🧊 27 | | <u>a P</u> | | | | | |
|------------------------|----------|------------------------|----------|----------|----------|--------------|------|
| esign Variables | | Outputs ? 🗗 | | | | | |
| | | Name/Signal/Expr | Value | Plot | Save | Save Options | T Si |
| Name V VDD 519.132r | Value _ | 1_X0 | | | | allv | Î |
| VEXT VDD | | 2 X1 | | | ¥ | allv | L |
| VEXT | ▲ | 3 X2 | | | V | allv | H |
| | | 4 X3 | | | ¥ | allv | 2 |
| 0 | .519V | 5 OUT | | | | allv | 0 |
| U | 0.3134 | 6 V0/MINUS | | 100 | ¥ | yes | (|
| | | 7 V0/PLUS | | | V | yes | (|
| | | 8 tplh_X0_OUT | 799.999p | | ¥ | | |
| | | 9 tphl_X0_OUT | 790.889p | | V | | 2 |
| | | 10 tplh_X1_OUT | 715.323p | | ¥ | | |
| | | 11 tphl_X1_OUT | 659.019p | | ¥ | | |
| | | 12 tplh_X2_OUT | 712.256p | V | | | |
| | | 13 tphl_X2_OUT | 730.352p | | V | | |
| | | 14 tplh_X3_OUT | 781.1p | | - | | |
| | | 15 tphl_X3_OUT | 779.448p | | | | |
| | | 16 Delay_X3_OUT | 780.274p | | | | |
| | | 17 Delay_X2_OUT | 721.304p | | ¥ | | |
| | | 18 Delay_X1_OUT | 687.171p | | - | | |
| | | 19 Delay_X0_OUT | 795.444p | | | | |
| (!) 95.8f | J | 20 Energy | 95.8411f | | | | |
| (., | | Plot after simulation: | Auto | | | Replace | 1 |

VDD scaled according to given testbench

Thanks for listening! $\checkmark(\bullet \omega \bullet^*)$